GHz Flip Chip - An Overview

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Abstract

The drive in industry towards more and more wireless communication for various purposes increases the need for packaging for ever higher frequencies. This paper gives an overview of recent activities, presented by companies and universities, at GHz frequencies. The main topic is the chip interconnect, and GaAs flip chip specifically.

Flip chip offers some very significant advantages over wire bonding, such as better electrical performance and smoother assembly process. This makes way for lower production costs and allows for low cost high volume production of both consumer and other products. For lower frequencies, this is well documented, and an increase in activity for high frequencies is now seen. If one is to judge by the number of papers presented, it seems that most of the activities are in USA, Europe, and Asia. In Europe, Germany presents the most results, and in Asia, various Japanese companies dominate. However, it is likely that most of the well known telecom and radar companies are actively investigating flip chip for high frequencies, without presenting the results.

Papers are mostly concerned with chip design issues, and simulations of various structures. The coplanar chip design appears to be favored, along with non-melting bumps for interconnect.

Introduction

High speed and microwave circuits are defined as digital circuits with clock speeds above 10 MHz and analog circuits operating at 0.1 to 100 GHz, respectively [1]. This of course requires careful consideration when selecting materials and creating the packaging for such a circuit.

There are several feasible alternatives for flip chip joining of GaAs chips for high frequency applications, and these are discussed, based on the information given in these papers. There are variations in for example materials and techniques for substrates, bumps, chip design, methods for simulation and production.

Flip Chip Interconnect Systems

The flip chip interconnect is based on three fundamental building blocks, the bumps on the chip, the substrate and the method of joining the chip to the substrate. These three are interdependent, and therefore it is important to see the full picture in order to select the flip chip system to be used for a specific application. In recent literature, many different high frequency flip chip systems are proposed.

Bumping

The bumping of GaAs is an example of a specific challenge in microwave flip chip. When using chemical bumping, the chemical that is selected to react with the gold on the chip pads will also react with the gold on the air bridges, which of course is not desirable. Furthermore, most users will not be able to obtain undiced wafers. The chips then have to be bumped as singulated die. Few options then remain, among these are bumping of the substrate, a process that has been described in papers by Alcatel in Germany. Another way to solve this may be to use stud bumping of the die by traditional wire ball bonding.

Wafer bumping is an additional process, performed before wafer scribing or sawing. GaAs chips are often thinned to enhance the thermal performance, because of the lower thermal conductivity of GaAs compared to Si (30 and 90 W/m K respectively). The yield in wafer fabrication is therefore lower, due to the handling of thin, brittle GaAs wafers. Typical values of the wafer thickness are 625 µm before and 127 µm after back grinding. The yield will certainly be even lower if the wafers have to travel through bumping. Some bumping houses state that they do not handle thinned wafers at all.

The chip interconnect pads for the III-V materials are gold, whereas the Si chips have Al pads. The ordinary tin/lead solders do not wet to Al, and a so called under bump metallurgy (UBM) is therefore needed. Solder does wet to gold, but the intermetallics formed in that system are not favorable to reliability, a well documented fact. Therefore, it may be necessary, or at least beneficial to use an UBM also for the III-V chips. An interesting approach to tin/lead bumping with small diameters comes from Hewlett-Packard [2], implemented for InP chips. The process includes TiWN, NiV and Au layers as UBM, and the 60/40 Sn/Pb solder is deposited by evaporation. Since the pad metallurgy of the InP and the GaAs is the same, it is likely that the process works for GaAs also. The bumps are set to be 30 µm diameter and 25 µm high.

Apart from the pad metallurgy, methods for flip chip bumping of GaAs are similar to the ones used for silicon. The plating methods dominate, such as electroplating and chemical plating. Also used are transfer bumping and stud bumping. Another way is to apply a solder or conductive adhesive paste to the board or to the bumps directly.

Alcatel presents an less common version of bumping where the substrate is galvanically gold bumped, as a part of the standard processing of four inch thin film substrates. A benefit with this approach is that the chips require no preprocessing.

Substrate

Most studies have selected alumina as a carrier for the chips. Alumina has a coefficient of thermal expansion (CTE) very similar to that of GaAs, and it is therefore very appropriate. It has also got good electrical properties, such as for the dielectric constant, ε, and the loss. Typical values for some substrate materials are given in Table 1. Please note that

many of the values are depending on the resin content of the material. The values are measured at 1 MHz unless otherwise stated.

Substrate type	Dielectric constant	Loss tangent, tan δ	In-plane CTE, (ppm/°C)
Pure PTFE [3] (60 GHz)	2.1	0.0001	100 - 120
PTFE with woven glass [4] (10 GHz)	2.2	0.0009	12 - 16
FR-4 [5]	4.2 - 4.5	0.025	12 - 16
Getek [6]	3.6 - 4.2	0.010 - 0.015	12 - 16
Alumina, Al_2O_3, 96% [7]	9	0.0006	7
Aluminum Nitride, AlN [7]	8 - 10	0.0007 - 0.002	4.5
Silicon Carbide, SiC [7]	40	0.05	3.7

Table 1. Properties of various substrate materials.

Chip Joining Method

The chip joining method is, of course, closely related to both bumping and substrate technology. Several methods are being tried out, such as thermocompression, thermosonic bonding, soldering, and adhesive joining.

Depending on the bump and substrate materials, the chip joining can be done in a number of ways. The most well known is *soldering*, using high or low melting point bumps. For low melting point bumps, the joining process is quite straightforward. The chip is placed in flux or solder paste on the substrate and the assembly is reflowed. The joint is formed through the melting of the actual bump, and the paste, where applicable. The high melting point bumps, also known as solid core bumps, is joined to the substrate by melting either solder paste or a low melting alloy on the bumps or on the conductors on the substrate. The chip to substrate stand-off is well defined and will be greater than or equal to the non-melting bump height.

Soldering is the most well known method, and it has some significant advantages. First of all, when soldering flip chips, the surface tension of the molten solder will pull the chip to its correct position, i.e., the chip self-aligns. This means that the mounting does not have to be extremely precise. The solder can only wet to the metal surfaces on the substrate, and as long as the chip bump is in contact with the correct pad on the surface, the chip will self-align. Trials with Si chips have shown that the chip can be dislocated as much as 50% of the pad diameter and still result in good alignment.

Other flip chip joining methods include *thermocompression*, where gold bumps and conductors are pressed together during heat exposure. A rule says that when the temperature reaches 300 °C, a Au bond can be formed without using ultrasonic energy [8]. The settings used in Alcatel's studies have changed over the years, [9, 10], to lower temperature and pressure.

At the University of Colorado, Boulder, a *thermosonic* flip chip bonding technique has been developed [11, 12]. It allows for bonding at lower temperature and pressures with ultrasonic energy added. The impact of the ultrasonic energy on the chip is investigated, to make certain that any adverse effects are under control.

Hughes appear to have chosen solid, non-melting silver bumps attached using tin solder or adhesive. Table 2 shows some of the selected bumping and joining schemes.

Company	Bump material, diameter (µm) & height (µm)	Substrate	Joining method
Alcatel [9, 10, 13, 14]	Au diameter >15 height 25 - 40	Al_2O_3	Thermo-compression
Fujitsu [15]	Au pillars diameter 40 height 20	Al_2O_3	AuSn solder
Hughes [16, 17, 18, 19, 20]	Ag diameter 150 height 100	AlN	solder reflow or conductive adhesive
Matsushita [21, 22]	Au transfer diameter 40 height 2 - 3	Si	insulating resin, compressive
NTT [23, 24]	In, InPb diameter 20 - 40 height 20 - 30	AlN	solder reflow
OKI [25]	Not stated diameter 80 height >30	Ceramic	Not stated
Sharp [26]	Au emitter 6 x 20 height unknown	AlN	Thermo-compression
TI [27, 28]	Au emitter 4 x 100 height unknown	Cu, CuMo	AuSn solder reflow
TRW [29]	hard/soft PbSn, diameter unknown height 100	Not stated	PbSn reflow

Table 2. Bumping, substrate and joining methods for some recent investigations.

Encapsulation

Perhaps the chip encapsulation can be considered the fourth flip chip building block. In the case of microwave circuits, the encapsulation, be it underfill or glob top, is considered detrimental to the electrical properties. The main reason that encapsulants are difficult is that they are not homogeneous. An encapsulant consists of a bulk material, often epoxy, and a filler, such as silica or silicon nitride. The uneven dielectric properties may or may not affect the

electrical performance of the circuit at a given frequency. However, there is hardly any point in creating an assembly which works perfectly electrically but cannot withstand storage or operation mechanically. The chips have to be protected in some way. Chemically, the chip passivation may be enough, but mechanical support is most likely needed, due to the difference in Coefficients of Thermal Expansion, CTE, between chip and substrate.

A recent study [30, 31] shows that the damping effect of underfill is actually less than that of glob top. The reason is that the glob covers more of the surrounding conductor patterns on the substrate than does the underfill. Underfill is pulled in under the chip and kept in place by the capillary action. The glob and underfill materials are quite similar apart from the difference in viscosity. Underfill is supposed to flow whereas glob top should stay in place once applied. Another paper [32] presents glob top used as underfill, where the low flow of the glob top is used as a beneficial feature. A cavity is left open under the chip in order to influence the electrical performance as little as possible. Full reliability testing is not reported, however.

Coplanar or Microstrip Chip Design?

Many studies involve a comparison between using coplanar and microstrip microwave flip chips. Today many chips are designed in a microstrip fashion, see Figure 1. TRW [29] has in a series of simulations, funded by GM-Hughes Electronics, shown how a microwave flip chip should be designed and assembled in order to minimize the effect of the mounting substrate on the performance of the chip. A coplanar structure, Figure 2, is said to be the most beneficial. As can be seen in the figures, it is more likely that the substrate will influence the field in the microstrip case than in the coplanar one.

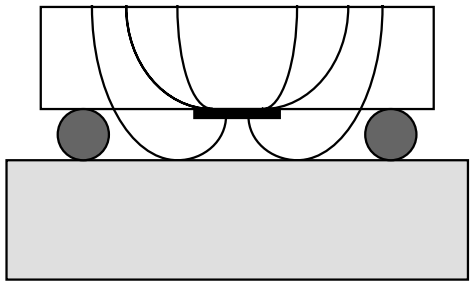

Figure 1. Field approximation for a microstrip flip chip.

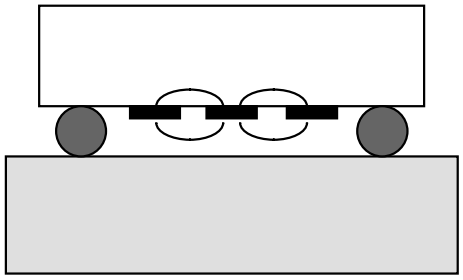

Figure 2. Field approximation for a coplanar flip chip.

Three fundamental parameters are said [29] to affect the interaction the most; the MMIC transmission line type, the spacing between the flip chip and the mounting substrate and the transition into the chip.

Interestingly, the optimum chip of substrate gap size is a topic of some debate. Alcatel claims that a 20 - 30 µm gap is the best, whereas TRW states that 102 µm gap size renders a field distribution which is independent of the substrate.

Chip Thinning?

As mentioned above, GaAs wafers are often thinned to enhance the heat conduction. By mounting the chip in a flipped manner, the heat can be transported directly from the heat generating structures on the chip down into the substrate.

Texas Instruments [28], Raytheon TI [27], Westinghouse [33], and Hughes [17] all propose enhanced cooling using flip chip bumps. The original H shaped heat sink bump concept was presented by Sharp [26], and it introduces the possibility to directly cool the heat generating structure by applying a gold bump on top of the transistor unit cell. Texas also proposes a non-flipped structure for very high heat dissipation, where via holes lead to the bumps which are on the backside of the chip. The chip is mounted face-up , connected by the bumps. This leaves the active side of the die towards the heat sink.

Table 3 attempts at giving an overview of the chip techniques used in the literature.

Company	**Frequency (GHz) meas.**	**calc.**	**chip type,**	**thinned (Y/N)**
Alcatel [9, 10, 13, 14]	75	--	CPW/µstrip MESFET, HEMT	Y
Fujitsu [15]	85	--	"MMIC"	--
Hughes [16, 17, 18, 19]	8 - 18	- 12	CPW MESFET	N
Hughes, SiGe [20]	- 18	--	µstrip HBT	N
Matsushita [21, 22]	30	75	µstrip HFET, HBT	--
NTT, InP [23, 24]	50, 60	90	CPW, --	--
OKI [25]	60	60	CPW PHEMT	Y (200 µm)
Sharp [26]	--	--	-- HBT	N
TI, power [28]	2	--	unflipped HBT	Y
Raytheon TI [29]	44	--	Embedded Transmission Lines	N
TRW [29]	--	50	CPW	N

Table 3. Frequency limits and chip design type for some recent investigations. Chips are GaAs unless otherwise stated.

Theoretical Evaluations And University Activities

Many universities and institutes are involved in simulations and calculations for high frequency flip chip [34, 35, 36, 37, 38, 39]. In some cases the theoretical work is complemented by actual measurements on flip chip structures. The trained eye will spot interaction with prominent companies in the same geographical area or area of interest. However, many companies perform their own simulations. As an example, an AT&T study [40] can be mentioned.

Selected Product Highlights

There are a few interesting applications that deserves to be mentioned. Most of the presented papers do not reveal their product application. Since most GHz bands are licensed for specific products, the reader can deduce from the stated operating frequency what the end product might be. Also the traditional product range of these companies should lead to some conclusions.

Alcatel is working on a glass antenna approach where the chip is interconnected to the back side of the antenna using a flip chip technique. The improvement in electrical performance over wire bonding is significant.

Fujitsu is indicating that its flip chip modules may be used in automotive radar systems.

Matsushita seems to be wanting to use its flip chip on Si modules for high performance packages. This also holds true for NTT, targeting optical communications.

High Frequency Silicon Flip Chips

Not all companies are interested in the very high frequencies requiring GaAs chips. Certainly, most packaging investigations concern the bands up to 2 GHz, for cellular phones. Recently, the bands up to 6 GHz have become the favorite topic, since that 5 - 6 GHz will be the standard band for wireless LAN products. These product types all have some features in common; they are produced in immense volumes, at low or moderate prices, and they are more or less portable. Therefore, flip chip becomes a natural packaging choice. For example, Philips is studying eutectic solder flip chips [41] for 1.9 GHz (cellular phone frequency), and Matsushita presenting a SAW filter [42] using their stud bump bonding (SBB) process. The SBB uses gold wire stud bumped chips. The chip bumps are dipped in conductive adhesive, the chip is mounted to ceramics, the adhesive cured. The process uses underfill and shows good results to 1.5 GHz.

Conclusions

Many of the large companies involved in telecom and radar communication are conducting research and development in the field of advanced chip interconnect. The benefits with flip chip over wire bonding are well documented for lower frequencies, and now there are a significant number of papers being presented on flip chip for RF, microwave, and millimeter wave applications. Judging from the number of papers published, the main activity in Europe seem to be going on at Alcatel, whereas in the USA, Hughes has presented the most papers on this topic. However, not all companies choose to reveal their intentions in that manner.

Some general conclusions dominate through most of the literature:

- The chips shall be designed in a coplanar fashion, in order to achieve the most beneficial field distribution, and to avoid interaction with the substrate.
- By using coplanar chips, the wafer back grinding, via hole generation and back plating of the chips can be avoided completely. This leads to a significant cost reduction due to the increase in yield, both at the wafer fabrication stage and in assembly.
- The overall electrical performance of flip chip mounted microwave chips is much better than that of equivalent wire bonded chips.

There are also disagreements in some basic fundamentals, for example:

- The optimum stand-off height (the chip-to-substrate gap) remains a topic of debate. Some studies state that 20 µm is the most beneficial, and others go as high as 100 µm, which is more common practice in today's silicon based flip chip.

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References

Since this paper aims at reflecting the ongoing research into GHz packaging, the reader will also find the affiliation of the authors listed for each article reference below, in addition to the regular reference information.

1 Konsowski, S. G., Helland, A. R., Electronic Packaging of High Speed Circuitry, McGraw-Hill (New York, 1997).

2 Tan, T. S., Kocot, C., Strazincky, J., Armistoso, M., "A Micro Flip Chip for High Speed Optoelectronic Components", *Proc. Surface Mount International*, 1996, Hewlett-Packard, Palo Alto, CA, USA.

3 Harper, C., Sampson, R., Electronic Materials and Processes Handbook, McGraw-Hill (New York 1994).

4 Taconic TLY5 product information

5 Isola product information

6 General Electric product information

7 Brown, R., Materials and Processes for Microwave Hybrids, ISHM (Reston, 1991).

8 Harman, G., Wire Bonding in Microelectronics - Materials, Processes, Reliability, and Yield, McGraw-Hill (New York, 1997).

9 Richter, H., Baumgärtner, A., Baumann, G., Ferling, D., "Flip Chip Attach of GaAs-Devices and Application to Millimeter Wave Transmission Systems", *Proc. MST - Micro Systems Technology*, Berlin, 1994, Alcatel, Pforzheim, Stuttgart, DE.

10 Buchali, F., Richter, H., Hierl, R., Gutu-Nelle, A., Florjancic, M., Ferling, D., "RF and thermal behaviour of flip chip mounted GaAs power devices", *Proc. Area Array Packaging Technologies*, Berlin, 1997, Alcatel, Pforzheim, Stuttgart, DE.

11 Kang, S.-Y., Williams, P. M., Lee, Y.-C, "Modeling and Experimental Studies on Thermosonic Flip-Chip Bonding", *IEEE Transactions on Components, Packaging,*

and Manufacturing Technology Part B: Advanced Packaging, November 1995, Volume 18, Issue 4, Univ. Colorado, Boulder, CO, USA.

12 McLaren, T., Kang, S.-Y., Zhang, W., Hellman, D., Ju, T.-H., Lee, Y. C., "Thermosonic Flip Chip Bonding for an 8 x 8 VCSEL Array", *Proc. 45th Electronic Components and Technology Conference*, 1995, Univ. Colorado, Boulder, CO, USA.

13 Baumann, G., Ferling, D., Richter, H., Baumgärtner, A., Müller, E., "Comparison of flip chip and wire bond interconnections and the technology evaluation on 51 GHz transceiver modules", *Proc. Area Array Packaging Technologies*, Nov. 1995, Alcatel, Pforzheim, Stuttgart, DE.

14 Baumann, G., Richter, H., Baumgärtner, A., Ferling, D., Heilig, R., Hollmann, D., Müller, H., Nechansky, H., Schlechtweg, M., "51 GHz frontend flip chip and wire bond interconnections from GaAs MMIC to a planar antenna", *Proc. IEEE MTT-S International Microwave Symposium*, 1995, Alcatel, Pforzheim, Stuttgart, Fraunhofer Inst., Neuburg, DE Electrovac, Klosterneuburg, AT.

15 Aoki, S., Someta, H., Yokokawa, S., Ono, K., Hirose, T., Ohasi, Y., "A Flip Chip Bonding Technology Using Gold Pillars for Millimeter Wave Applications", *IEEE MTT-S International Microwave Symposium* 1997, Fujitsu Labs, Atsugi, JP.

16 Felton, L. M., "High yield GaAs Flip-chip MMICs lead to low cost T/R modules", *Proc. IEEE MTT-S International Microwave Symposium*, 1994, Hughes, Fullerton, CA, USA.

17 Cameron, P., Pan, W., Hanz, C., Nicklaus, R., Chu, P., Wong, D., Cisco, T., "A Flip-Chip High Efficiency X-Band HPA", *Proc. IEEE MTT-S International Microwave Symposium*, 1997, Hughes, Fullerton, Torrance, El Segundo, CA, USA.

18 Bao, J.W., Wei, C. J., Hwang, J. C. M., "Pulsed Internal-Node Waveform Study of Flip-Chip MMIC Power Amplifiers", *IEEE MTT-S International Microwave Symposium*, 1997, Lehigh Univ. Bethlehem, PA, Hughes, Torrance, USA.

19 Marks, B., Jargon, J. A., Pao, C. K., Wen, C. P., "Microwave Characterization of Flip Chip MMIC Components", *45th Electronic Components and Technology Conference*, 1995, NIST - National Institute of Standards and Technology, Boulder, Co., Hughes, Torrance, CA, USA.

20 Case, M., "SiGe MMICs and Flip-Chip MICs for Low-Cost Microwave Systems", *Proc. IEEE MTT-S International Microwave Symposium*, 1997, Hughes, Malibu, CA, USA.

21 Takahashi, K, Fujita, S., Yoshida, T., Sakai, H., Sagawa, M., "An Advanced Millimeter-Wave Flip-Chip IC Integrating Different Kinds of Active Devices", *IEEE MTT-S International Microwave Symposium*, 1996, Matsushita, Kawasaki, JP.

22 Sakai, H., Ota, Y., Inoue, K., Yoshida, T., Takahashi, K., Fujita, S., Sagawa, M., "A Novel Millimeter-Wave IC on Si Substrate using Flip-Chip Bonding Technology", *Proc. IEEE MTT-S International Microwave Symposium*, 1994, Matsushita, Osaka, JP.

23 Tsunetsugu, H., Hayashi, T., Katsura, K., Hosoya, M., Sato, N., Kukutsu, N., "Accurate, stable, high-speed interconnections using 20- to 30-µm-diameter microsolder bumps", *IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part A*, vol. 20, no. 1, March 1997, NTT Opto-electronics Labs, Tokyo, NTT Telecommunications Networks Labs, Kanagawa, JP.

24 Yamaguchi, S., Imai, Y., Kimura, S., Tsunetsugu, H., "New Model Structure Using Flip-Chip Technology for High-Speed Optical Communication ICs", *IEEE MTT-S International Microwave Symposium*, 1996, NTT LSI Labs, NTT Interdisciplinary Labs, JP.

25 Arai, Y., Yamada, H. T., Hamada, T., Nagai, K., Fujishiro, H. I., "60 GHz Flip-Chip Assembled MIC Design Considering Chip-Substrate Effect", *Proc. IEEE MTT-S International Microwave Symposium*, 1997, OKI Electric Industry Co., Tokyo, JP.

26 Sato, H., Miyauchi, M., Sakuno, K., Akagi, M., Hasegawa, M., Twynam, J. K., Yamamura, K., Tomita, T., "Bump heat sink technology - a novel assembly technology suitable for power HBTs", *Proc. GaAs IC Symposium*, 1993, Sharp Corporation, Nara, JP.

27 Tserng, H.-Q., Saunier, P., Ketterson, A., Witkowski, L. C., Jones, T., "Embedded Transmission-Line (ETL) MMIC for low-cost high-density wireless communication applications", *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 12, December 1997, Raytheon TI Systems, Dallas, TX, USA.

28 Hill, D., Kim, T. S., "28-V low thermal-impedance HBT with 20-W CW output power", *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 12, December 1997, Texas Instruments, Dallas, TX, USA.

29 Sturdivant, R., "Reducing the effects of the mounting substrate on the performance of GaAs MMIC flip chips", *Proc. IEEE MTT-S International Microwave Symposium*, 1995, TRW , Redondo Beach, CA, USA.

30 Baumann, G., Müller, E., Buchali, F., Ferling, D., Florancic, M., Heck, W., Richter, H., "Low Cost Packaging of Millimeter Wave Devices", *Proc. Area Array Packaging Technologies*, Berlin, 1997, Alcatel, Pforzheim, Stuttgart, DE.

31 Baumann, G., Müller, E., Buchali, F., Ferling, D., Richter, H., Heinrich, W. "Evaluation of Glob Top and Underfill Encapsulated Active and Passive Structures for Millimeter Wave Applications", *Proc. 27th European Microwave Conference*, Jerusalem, 1997, Alcatel, Pforzheim, Stuttgart, Ferdinand-Braun Institute, Berlin, DE.

32 Sturdivant, R., Quan, C., Woolridge, J., "Investigation of MMIC flip chip with sealants for improved reliability without hermeticity", *Proc. IEEE MTT-S* 1996, Hughes, El Segundo, CA, USA.

33 Bayraktaroglu, B., Ali, F., Mason, J., Smith, P., “Flip-Chip X-Band Operation of Thermally-Shunted Microwave HBT’s with Sub-Micron Emitters”, *Proc. IEEE MTT-S International Microwave Symposium*, 1996, Westinghouse, Baltimore, MD, USA.

34 Ghouz, H., El-Sharawy E.-B., “An Accurate Equivalent Circuit Model of Flip Chip Interconnects”, *Proc. IEEE MTT-S International Microwave Symposium* 1996, Arizona State Univ., Tempe, USA.

35 Gilbert, B. K., Pan, G-W, “MCM packaging for present- and next-generation high clock-rate digital - and mixed-signal electronic systems: areas for development”, *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 10, October 1997, Mayo Foundation, Univ. Tempe, AZ, USA.

36 Jackson, R. W., Ito, R., “Modeling millimeter-wave IC Behaviour for flipped-chip mounting schemes”, *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 10, October 1997, Univ. Massachusetts, Amherst, MA, USA.

37 Jin, H., Vahldieck, R., Minkus, H., Huang, J., “Rigorous field theory analysis of flip-chip interconnections in MMICs using the FDTLM Method”, *Proc. IEEE MTT-S International Microwave Symposium*, 1994, Univ. Victoria, MPR Teltech, Canada.

38 Krems, T., Haydl, W. H., Massler, H., Rüdiger, J., “Advantages of Flip Chip Technology In Millimeter-Wave Packaging, *Proc. IEEE MTT-S International Microwave Symposium* 1997, Fraunhofer Inst., Freiburg, DE.

39 Krems, T., Haydl, W. H., Massler, H., Rüdiger, J., “Millimeter-Wave Performance of Chip Interconnections Using Wire Bonding and Flip Chip”, *Proc. IEEE MTT-S International Microwave Symposium 1996*, Fraunhofer Inst., Freiburg, DE.

40 Rainal A., “Performance Limits of Electrical Interconnections to a High-Speed Chip”, *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, September 1988, Volume 11, No 3, AT&T Bell Labs, Whippany, NJ, USA.

41 Baggerman, A., Caers, J., Wagermans, A. G., “Flip Chip Mounting of an RF IC Using Eutectic Solder Bumps”, *Proc*. *Area Array Packaging Technologies*, Berlin, 1995, Philips CFT, Eindhoven NL

42 Onishi, K., Seki S-i., Taguchi Y., Bessho Y., Eda K., Ishida T., “An application of a flip-chip-bonding technique to GHz-band SAW filters for mobile communication”, *IEICE Trans. Electron.*, vol. E76-C, no. 6, June 1993, Matsushita Electric, Kadoma-shi, JP.